IDF15
INTEL DEVELOPER FORUM

Technology Insight: Intel's Next Generation Microarchitecture Code Name Skylake

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SPCS001

intel
experience what's inside™

AGENDA

Introduction and Overview

Core Microarchitecture

Interconnect and Memory

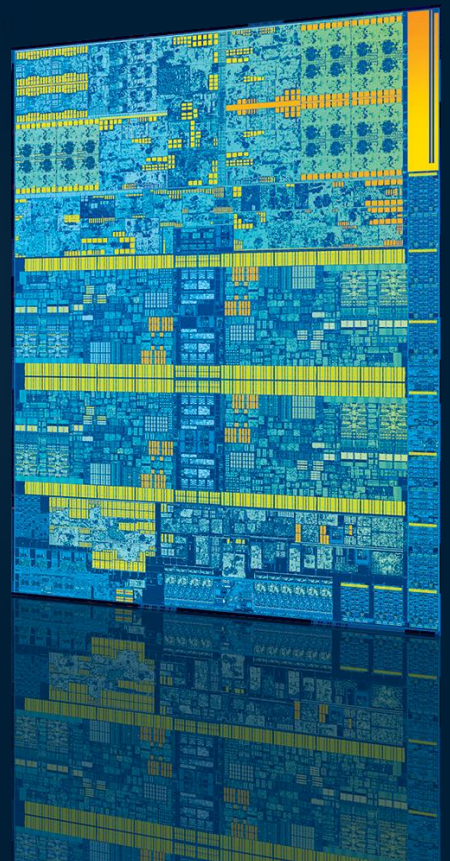
Power and Thermal

Other IPs and Technologies

Chipset Highlights

Overclocking

Summary and Q&A



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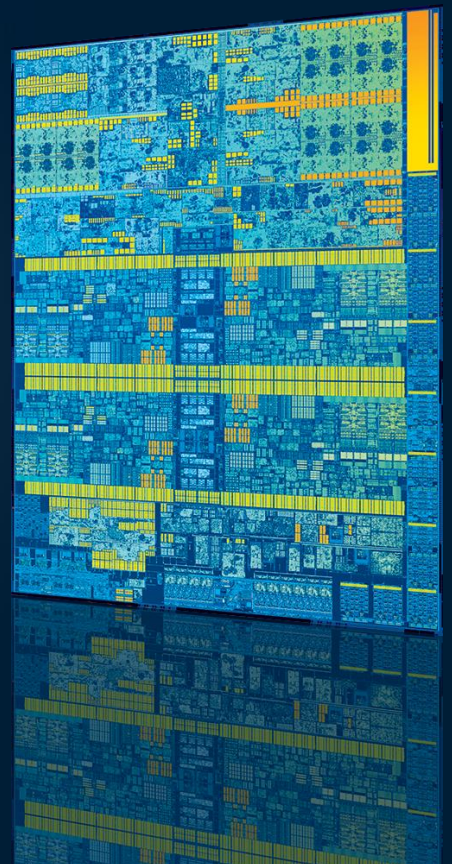


WHAT IS SKYLAKE?

USING 14NM BENEFITS TO DELIVER NEW MICROARCHITECTURE IMPROVEMENTS FOR CLIENT AND SERVER

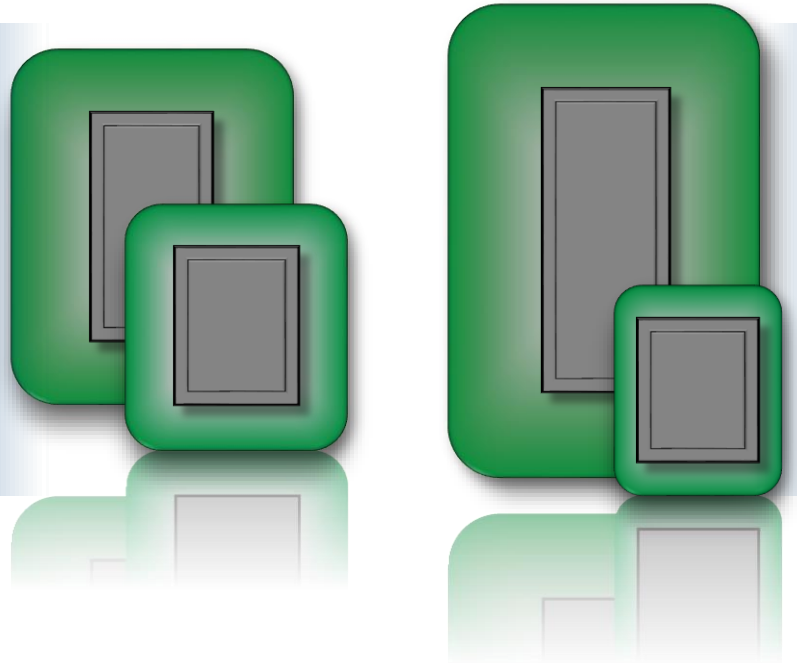
Skylake Development Adventure

Start

3x TDP scale

2x form factor range

Classic PC IO set



Finish

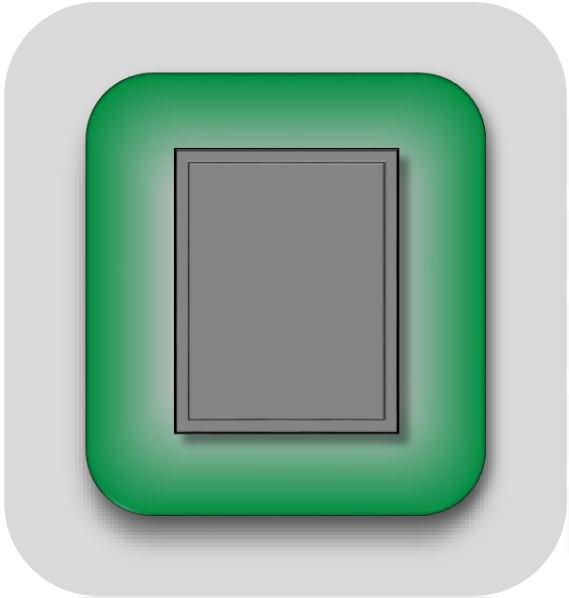
20x TDP scale

4x form factor range

Both PC and tablet I/O set

40%-60% less SoC power on video, multimedia, win-idle

Product Development Vectors



- Form factor reduction
- Support small form factor platforms
- Battery life scenarios power reduction and energy efficiency
- Continues Intel® Architecture performance improvement
- Improved GFX performance and multimedia capabilities
- New security technologies

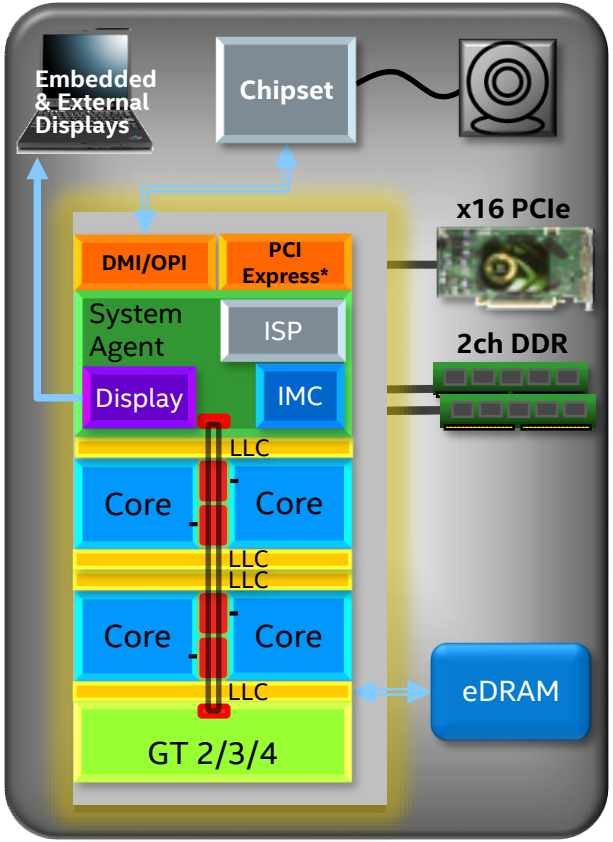
Intel's Skylake Microarchitecture

Increased chipset I/O throughput, Tablet I/Os, Audio DSP Upgrade, Sensor Hub

Higher resolution display

Bigger/wider core, better instruction per clock, improved power efficiency

Enhanced ring/LLC for improved throughput



Integrated camera ISP

Extended overclocking capabilities

Faster DDR Memory

Advanced Processor Graphics GT3 + eDRAM, GT4 + eDRAM; OpenCL™ 2.0 API, DirectX® 12, OpenGL* 4.4

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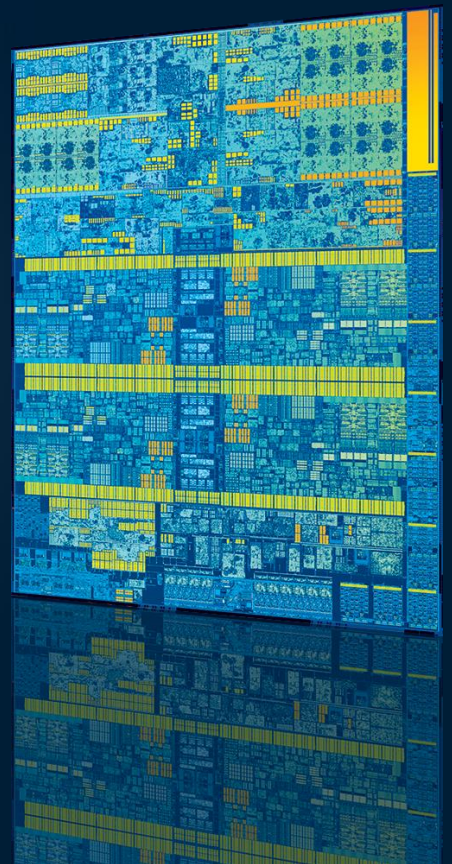
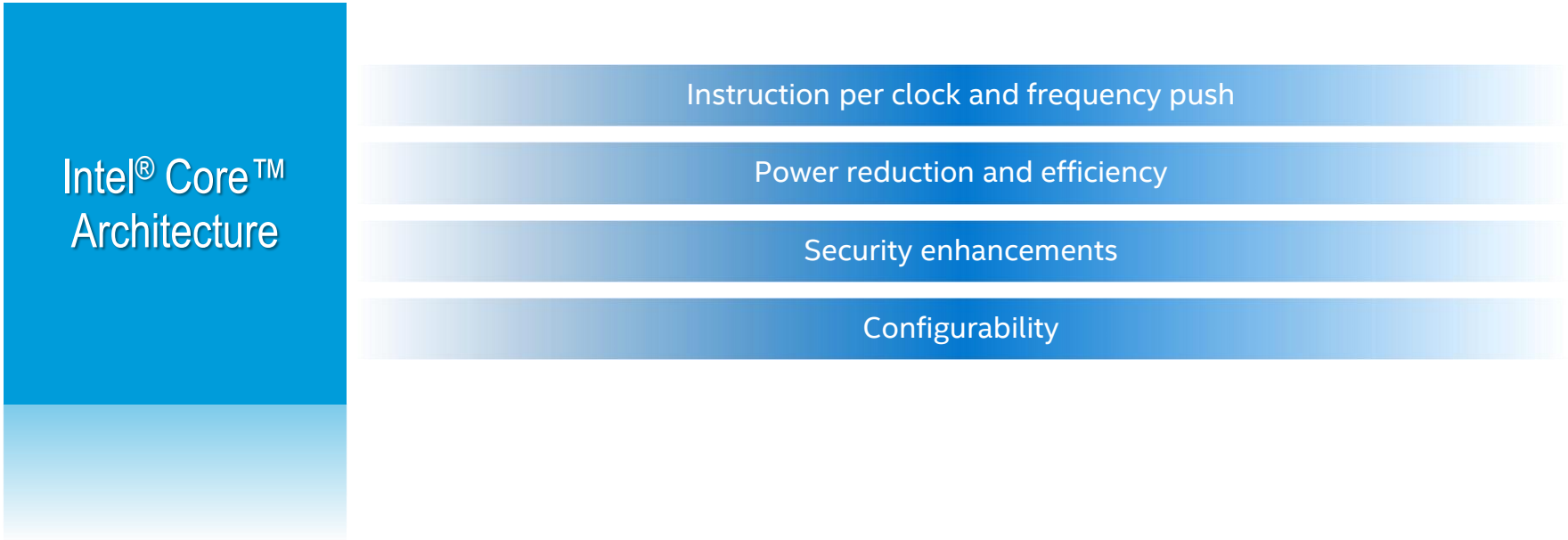


Core Microarchitecture Development Vectors



SKL Core Microarchitecture at a Glance (1 of 2)

Segment optimization

- Dedicated server and client IP configurations

Improved front-end

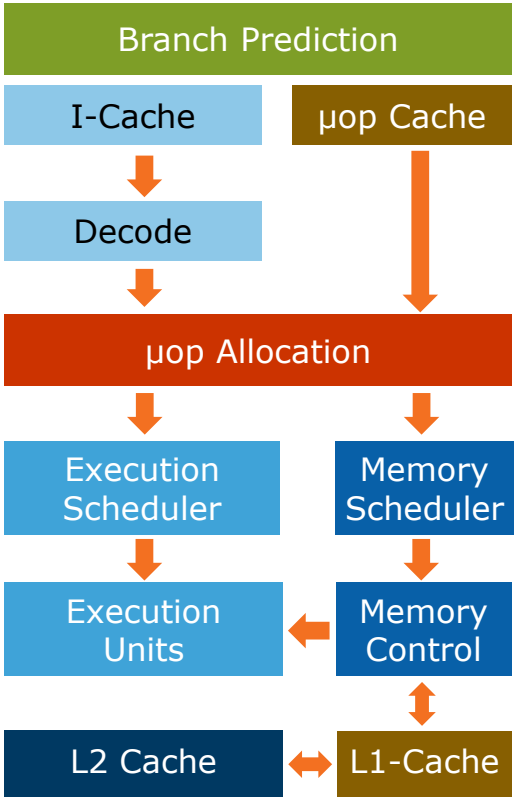
- Higher capacity, improved Branch Predictor
- Wider Instruction supply with deeper buffers
- Faster prefetch

Deeper Out-of-Order buffers

- Extract more instruction parallelism

Improved execution units

- Shorter latencies
- More units
- Power down when not in use
- Speedup of AES-GCM and AES-CBC by 17% and 33% accordingly



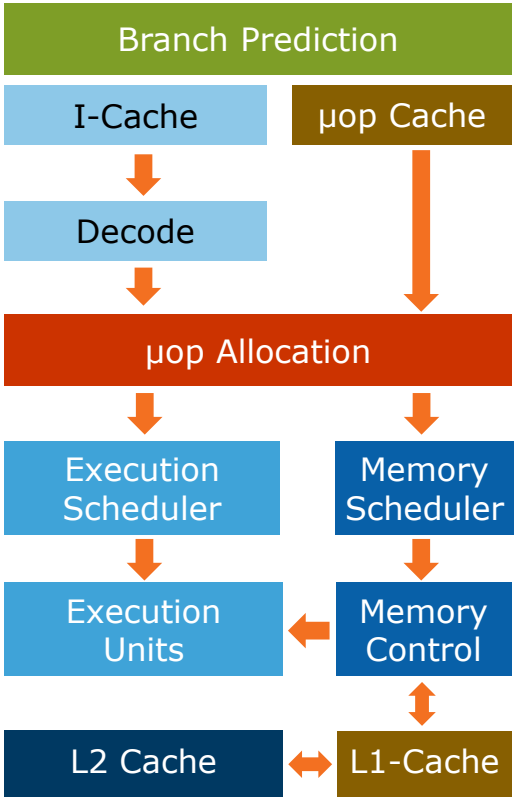
SKL Core Microarchitecture at a Glance (2 of 2)

More load/store bandwidth

- Prefetcher improvements
- Deeper store buffer, fill buffer and write-back buffer
- Improved page miss handling
- Better L2 cache miss bandwidth
- New instructions for better cache management

Improved Hyper-Threading

- Wider retirement



Instruction Window Keeps Increasing

	Sandy Bridge	Haswell	SkyLake
Out-of-order Window	168	192	224 ↑
In-flight Loads	64	72	72
In-flight Stores	36	42	56 ↑
Scheduler Entries	54	60	97 ↑
Integer Register File	160	168	180 ↑
FP Register File	144	168	168
Allocation Queue	28/thread	56	64/thread ↑

Extract more parallelism in every generation

New Security Technologies

- Skylake core supports Intel® Software Guard Extensions (Intel® SGX) technology
  - Supports new instructions and flows to create and isolate enclaves from malware and privileged software attacks
  - Enables usage of trusted memory regions (trusted enclaves)
- Intel® Memory Protection Extensions (Intel® MPX) implementation
  - Memory (both stack and heap) buffer boundary testing prior to memory accesses, to ensure the physical memory access falls within the bounds of the memory allocated to the calling process

Power Optimizations in the SKL Core

- Dynamic consumption based resource configuration
  - Power Gating of Intel® AVX2 (Intel® Advanced Vector Extensions 2) hardware when it is not used
  - Downscaling of underused resources
- Improved scenario based power (e.g. media playback) for great mobile experience
  - Idle power reduction
  - C1 state power reduction: improved dynamic capacitance (C_{dyn})

Better performance/Watt for the core, including focus on power at low utilization

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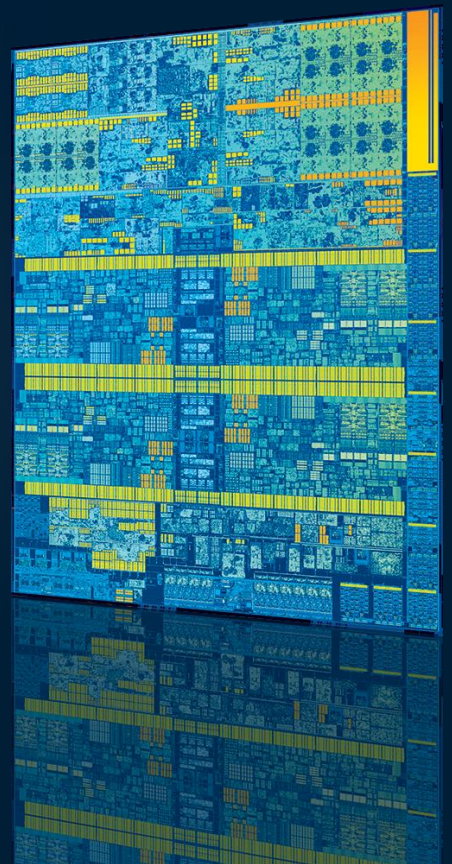
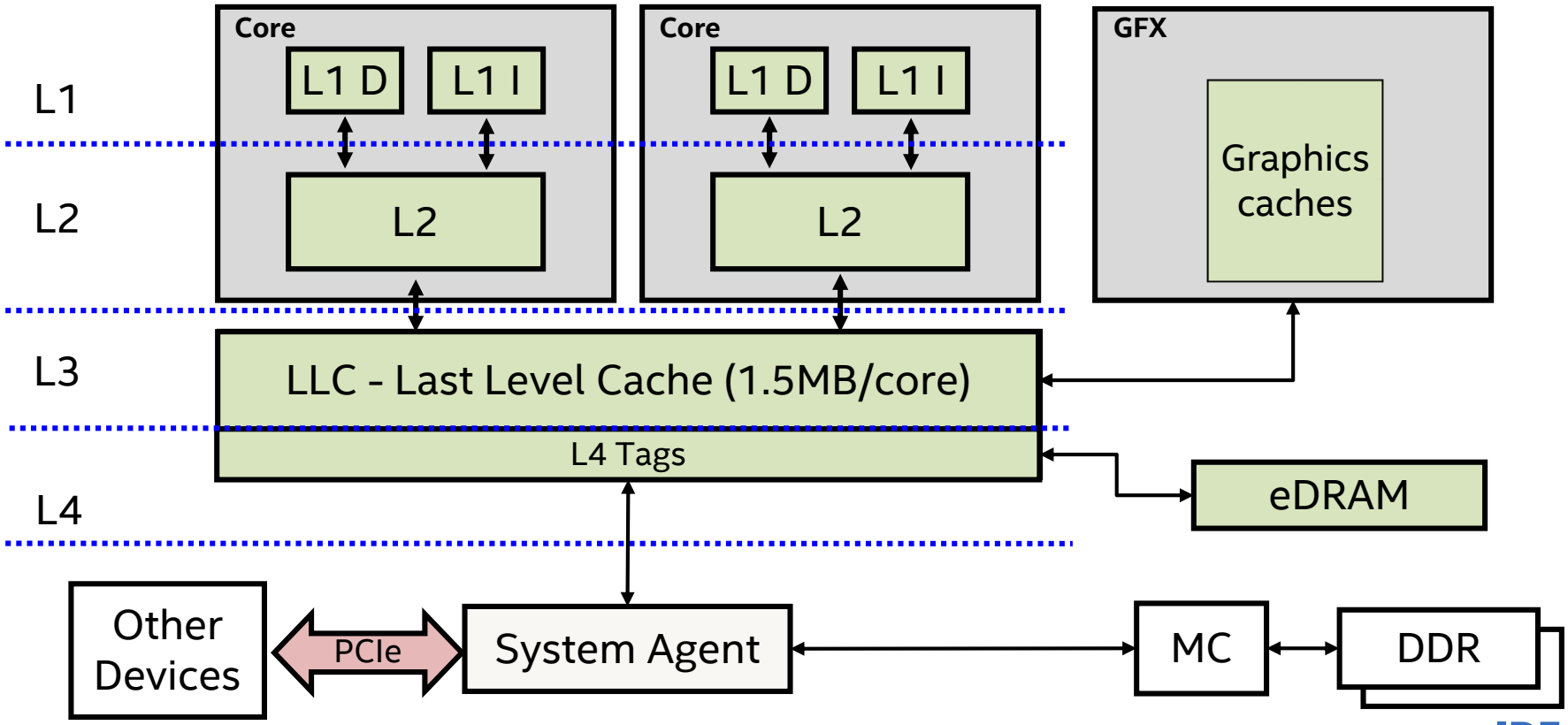


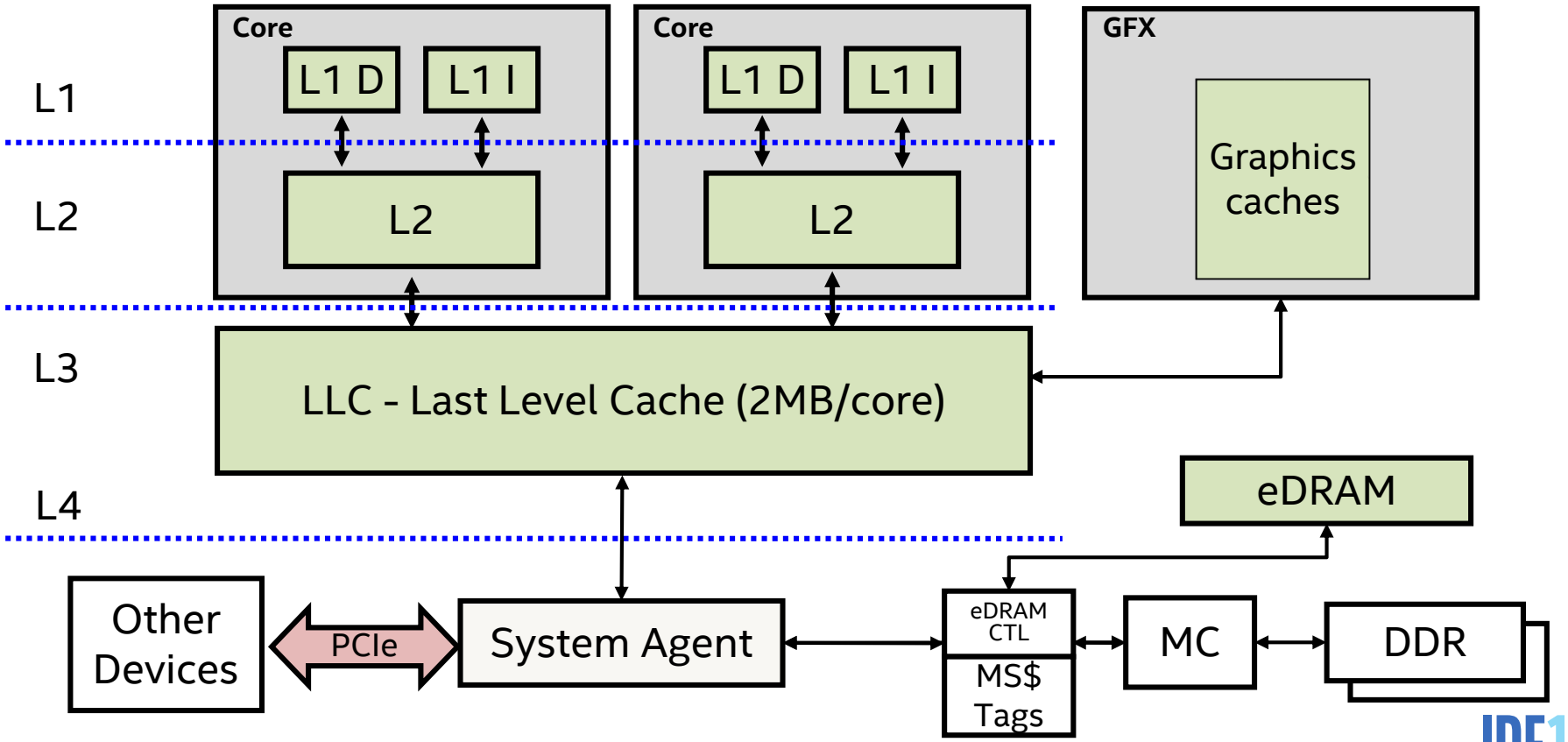
Next Generation Cache and Memory Solutions

- Double throughput of the last level cache (LLC) miss handling
- Fabric throughput was doubled without sacrificing power
- New eDRAM cache architecture, more products with eDRAM
- Support of faster DDR memory
- Main memory security and integrity engine
  - Used for Intel® Software Guard Extension (Intel® SGX) and other security-critical data
- Improved memory QoS for high resolution displays and integrated image signal processor (ISP)

eDRAM Based Cache



eDRAM Based Cache



eDRAM as Memory Side Cache

- Observed by all memory accesses, i.e. fully coherent
- Not architectural; can cache any data including “uncacheable memory” types
- No need to flush it for coherency maintenance
- Available for use by I/O devices and Display engine
- For optimal performance GFX driver may choose caching of particular data in the eDRAM only and not in the LLC

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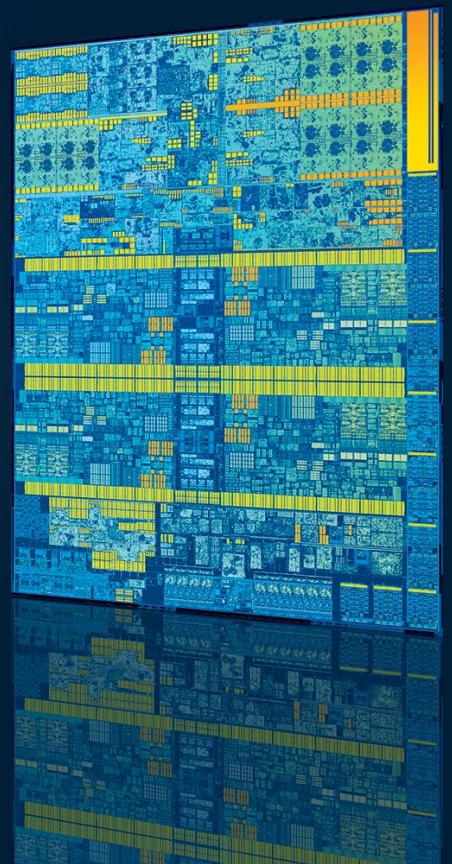

Power Reduction

Same process as Broadwell requires microarchitecture and design innovation to further reduce active and average power

- Reductions in every part of interconnects, inside IPs, I/O, PLLs etc.
- Drastic power reduction vs. previous generation SoC power in video playback, multimedia, and win-idle
- Low power support of high resolution panels (example: 25x14 -> 32x18: 1.6x pixels but only 1.2x power)
- More active power budget remains for real compute on IA/GT in power limited form factors (especially in fanless designs)

Optimized Energy Efficiency

- **Intel® Speed Shift Technology** OS hints about energy/performance preference. H/W performs the actual P-state control (autonomous)
  - Optimized frequency selection for low residency workloads, no longer a static knee point (*Race to Halt)*
  - Optimized frequency selection for best energy to performance trade offs
  - Kick down frequency (from idle) for best responsiveness while taking energy consumption into account
- **Duty Cycle Control** of the cores to reduce leakage power on very low power envelops while providing higher frequency and overall performance

Voltage and Thermal Optimizations

- More Intel® Speed Step Technology domains: System Agent, DDR and eDRAM I/O. Provide better performance on low bandwidth usages by increasing cores and/or graphics frequency on the account of the system agent and memory subsystem
- Provide skin temperature control services to the OEM
- Better thermal control on high junction temperature workloads, provide smooth frequency and much lower throttling

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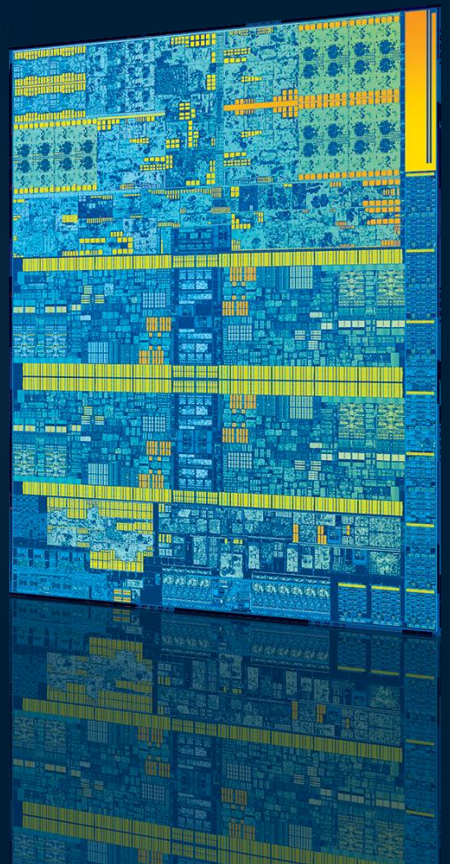
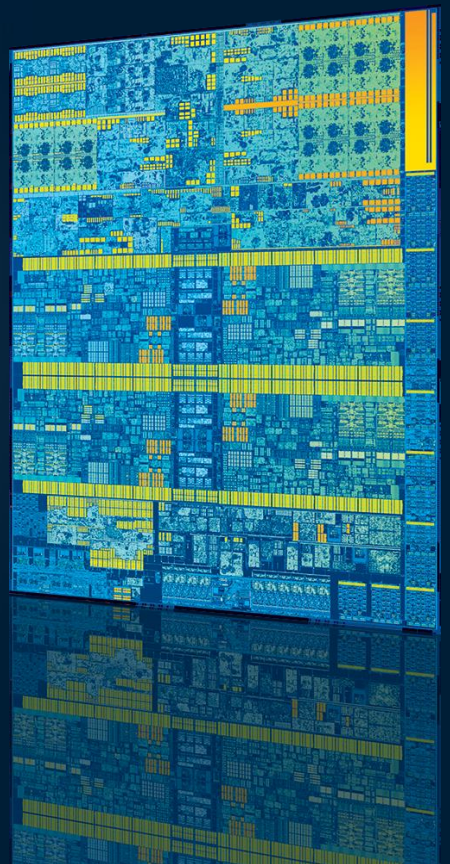
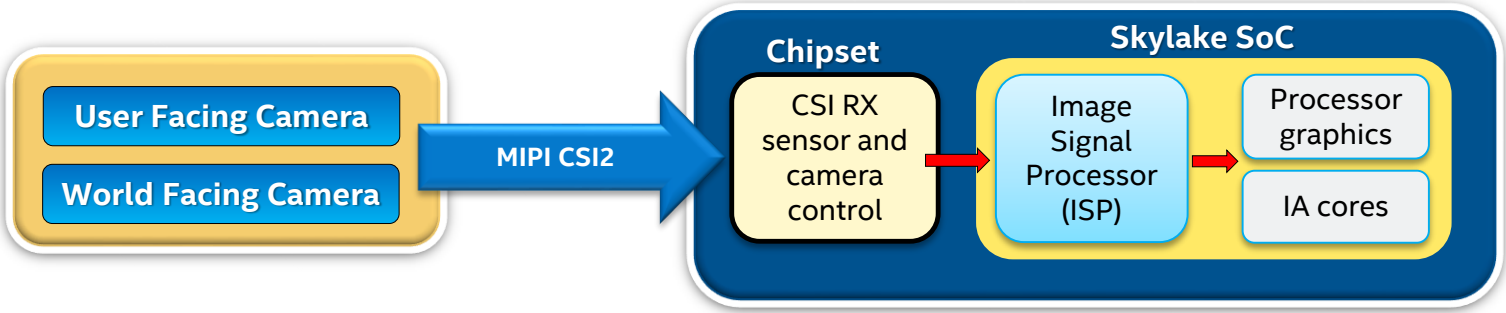


Integrated Image Signal Processor



Intel Next Generation Microarchitecture Code Name Skylake

Imaging Solution in Skylake



Complete Imaging & Camera Solution

- Full hardware and software integration
- Optimized module/sensor support:
  - Support up to 4 cameras (2 concurrent)
  - Up to 13MP sensors
- Premium quality imaging optimized system (ISP+ CPU + GPU + display)
- Partnerships with sensor ecosystem for TTM, reduced engineering costs, smaller form factors

Integrated ISP for Greater Efficiency

- BOM reduction
- Reduced module footprint
  - Enables smaller and thinner form factors
- Power optimized
- Enables advanced imaging and camera features

CSI = Camera Serial Interface

Skylake ISP Advanced Capabilities

Face Detection and Recognition
Smart Shutter (smile, blink)
Group Photo

13MP Zero Shutter Lag
Low power, high performance
1080p60 / 2160p30 video capture
Premium Image Quality

HDR
Ultra Low Light Capture

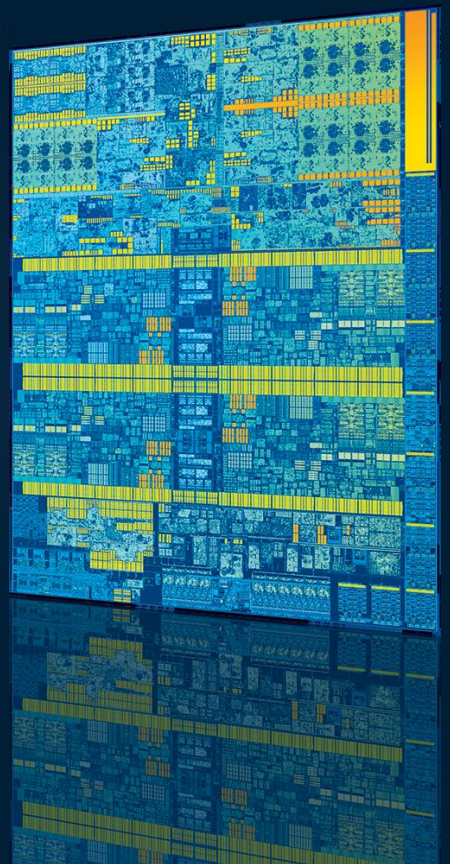
Burst Capture
Zero shutter lag (13MP)

Full resolution still capture during
video recording

Multi-stream Video capture
(2 concurrent streams)

Panorama

Intel® Software Guard Extensions (Intel® SGX)



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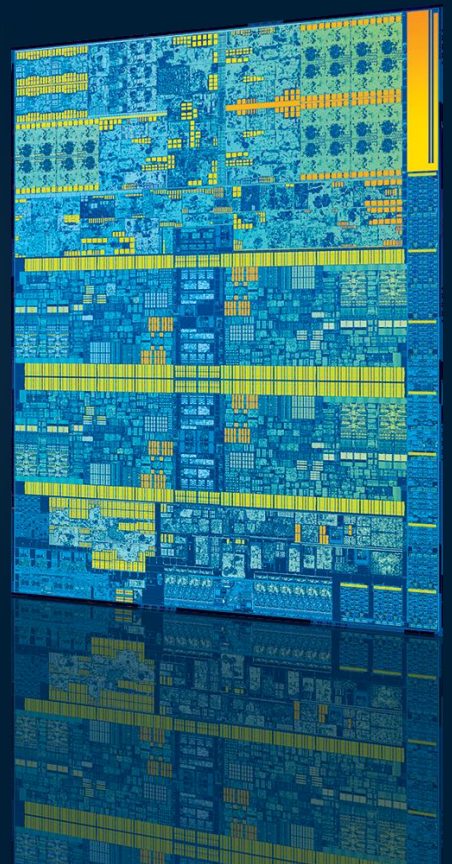
Intel® Software Guard Extensions (Intel® SGX)

- New instructions for creating and launching application-level trusted execution environments (TEE). Each instance of such an environment is called an enclave
- Allow any application to keep a secret
  - A secret can be code, data or both.
- Provides for integrity and confidentiality
  - Helps against software attacks, including privileged/kernel software
  - Protects against most hardware attacks. Enclave's DRAM protected against SW and HW attacks (integrity protection)
  - If trusted code is compromised, it will not launch
  - Protected secret cannot be retrieved via processor debug tools (e.g. ITP)

Graphics Media and Display Details in Follow-On Session:

SPCS003 “Next Generation Intel® Processor Graphics Architecture for Tablet, Client, and Workstation”
In this same room starting at 1:15pm today



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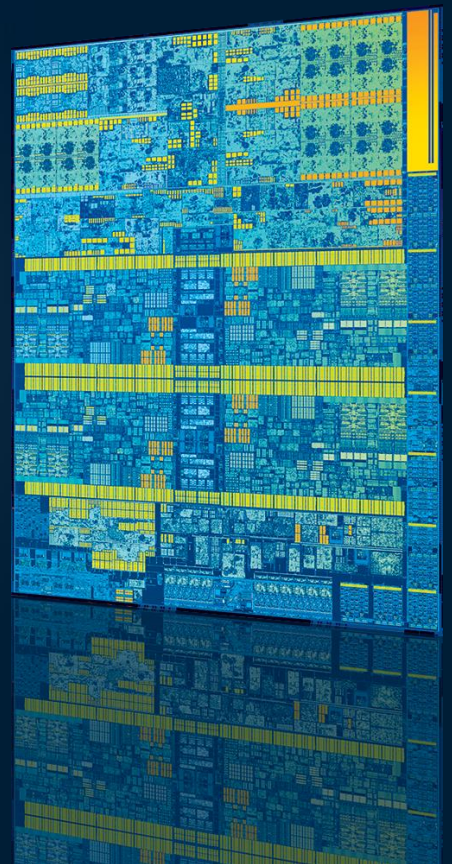

Skylake Chipset Family

- Power efficiency through new features such as HW autonomous power gating with retention flops, on-die power meter and throttling
- I/O focus:
  - Low power I/Os: eMMC, UFS, SDXC, CSI-2 for camera ISP in mobile SKUs
  - PCIe® and DMI upgraded to Gen3
  - More high speed I/Os (configurable as PCIe/SATA/USB3)
- Innovations:
  - Continued focus on Audio
  - Integrated Intel® Sensor Solution hub

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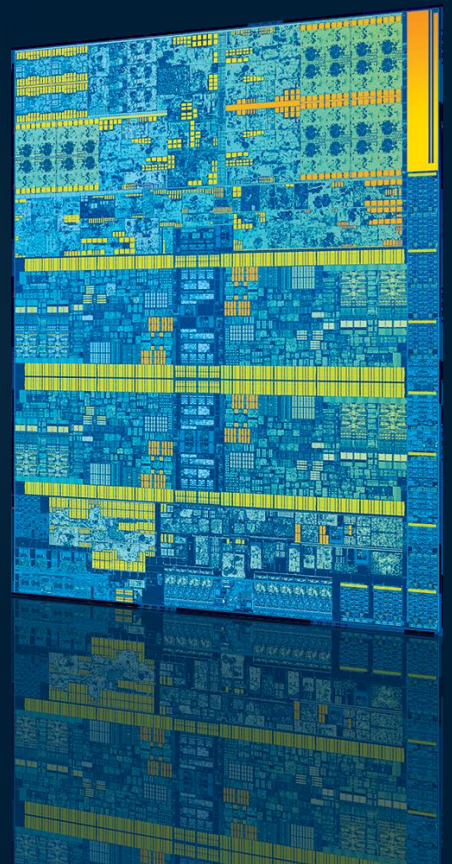
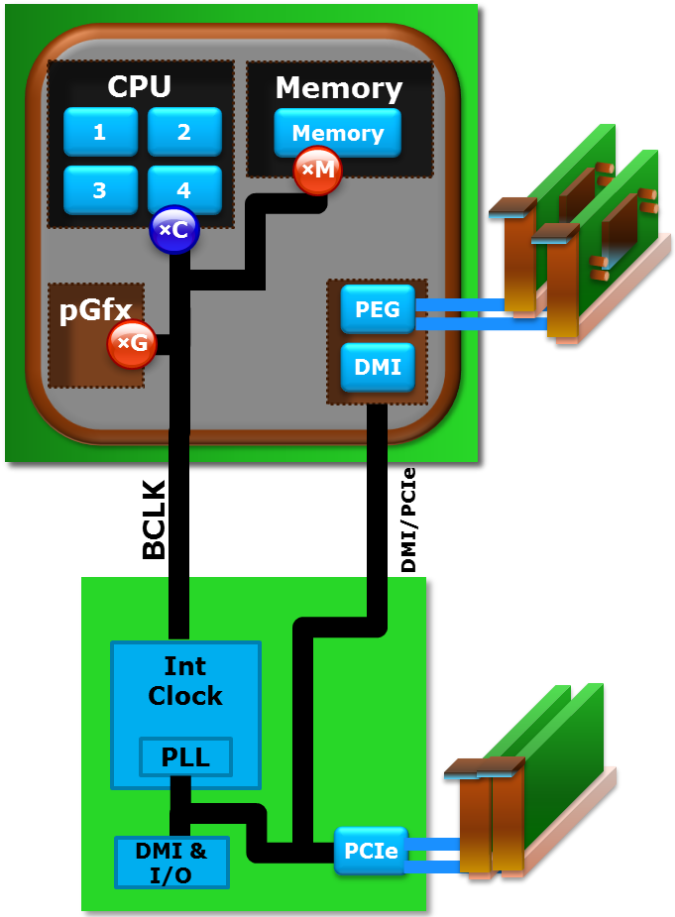


Overclocking Architecture Overview



- **×C Core Frequency**
  - Unlocked core ratios up to 83 in 100MHz increments†
  - Complete Turbo overrides for Voltage, Power Limits, IccMax
- **×G Graphics Frequency (pGfx)**
  - Unlocked graphics ratios up to 60 in 50MHz increments†
  - Turbo Voltage controls
- **×M Memory Ratio**
  - Options for 100 and 133 MHz steps†
  - Logical ratios up to at least 4133 MHz†
- **BCLK**
  - Separated from PCIe clock
  - Chipset clock controller
  - 1MHz increments
  - Up to 200 MHz or higher†
  - Note: Discrete clocking solutions exist which support finer than 1MHz increments and ranges far >250MHz †

† Subject to change at any time. Overclocking results not guaranteed.

Extreme Overclocking Achievements

Achieved on launch day†

SKYLAKE LAUNCH: 7 WORLD RECORDS, 10 GLOBAL FIRST PLACES

	BENCHMARK		SCORE	OVERCLOCKER	MOTHERBOARD	MEMORY
WR	PiFast		9,47	dRweEz	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
WR	3DMark05		78917	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
WR	3DMark06		61613	der8auer	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
WR	3DMark2001 SE		199091	elmor	ASUS Maximus VIII Gene	G.SKILL Ripjaws 4
WR	Aquamark		596039	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
WR	3DMark03		307658	der8auer	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
WR	Unigine Heaven - Xtreme Preset		9511,916	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	3DMark03	1xGPU	294423	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	Cinebench - R11.5	4xCPU	15,83	der8auer	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	Cinebench - R15	4xCPU	1410	dRweEz	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	Geekbench3 - Multi Core	4xCPU	27271	dRweEz	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	GPUPI for CPU - 1B	4xCPU	241,055	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	HWBOT Prime	4xCPU	7675,29	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	wPrime - 1024m	4xCPU	98,967	der8auer	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	wPrime - 32m	4xCPU	3,152	der8auer	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4
GFP	XTU	4xCPU	1731	FUGGER	ASUS Maximus VIII Gene	HyperX Predator
GFP	Unigine Heaven - Xtreme Preset	1xGPU	7619,562	Dancop	ASUS Maximus VIII Extreme	G.SKILL Ripjaws 4

(Table as of August 5, 2015. Source: hwbot.org database)

†Source: HWBOT article dated 2015-08-07
http://hwbot.org/newsflash/2983_skylake_the_day_after_7_world_records_and_10_global_first_places

Frequency Standings using Liquid Nitrogen†

- 4-Core @ 6.8 GHz
- DDR4 @ 4,795MT/s
- BCLK @ 552 MHz

Disclaimer: These overclocking results are not typical. Scores were achieved by extreme overclockers using LN2 and other advanced techniques not commonly available to average consumers. Overclocking results are not guaranteed nor covered by warranty. Extreme risk taking!

Rankings change regularly. Visit HWBOT's website for the latest http://hwbot.org

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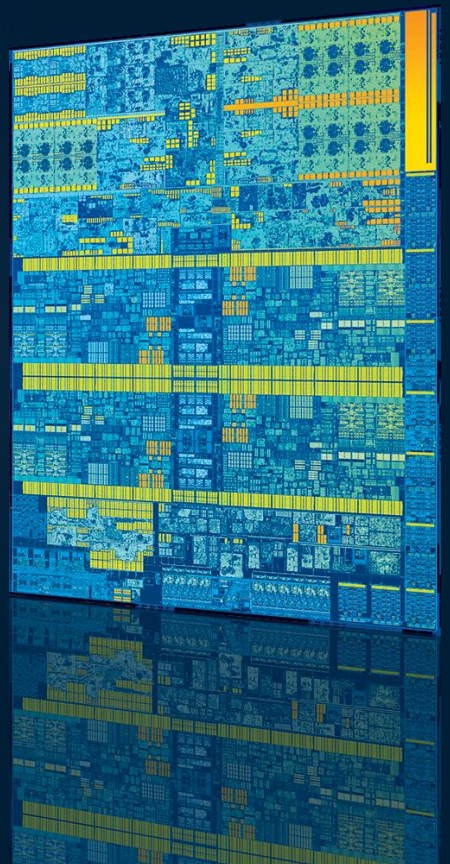

Summary and Next Steps

- The new Skylake SoC delivers record level performance and user experience into small form factor personal computing
- Our new product opens for product developers an ability to choose from wide range of platform capabilities and to develop optimal products for wide range of thermal envelopes and IO solutions
- Skylake introduces exciting overclocking capabilities

Additional Sources of Information

- A PDF of this presentation is available is available from our Technical Session Catalog: www.intel.com/idfsessionsSF. This URL is also printed on the top of Session Agenda Pages in the Pocket Guide.

Other Technical Sessions

	Session ID	Title	Day	Time	Room
✓	ARCS001	Intel® Architecture, Code Name Skylake Deep Dive: A New Architecture to Manage Power Performance and Energy Efficiency	Tues	2:30	2009
✓	ARCS002	Software Optimizations Become Simple with Top-Down Analysis Methodology on Intel® Microarchitecture, Code Name Skylake	Tues	2:30	2006
✓	SPCS003	Technology Insight: Next Generation Intel® Processor Graphics Architecture, Code Name Skylake	Tues	1:15	3016
✓	SPCS012	Zoom-in on Your Code with Intel® Processor Trace and Supporting Tools (No PDF available or audio)	Tues	5:30	Showcase Networking Plaza
✓	ARCS003	Intel® Architecture Code Name Skylake Deep Dive: Hardware-Based Security for Windows® 10	Tues	4:00	2006

✓ = DONE

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